

IN THE CLAIMS:

Please enter the following claims:

1. (currently amended) A method of testing an integrated circuit structure comprising the steps of:
providing a semiconductor wafer containing a set of chip locations for forming a set of integrated circuits therein;
fabricating in said wafer a set of transistors specific to a particular integrated circuit in said chip locations;
before electrical completion of said integrated circuit, connecting at least one subset of said set of transistors by a lithographic process in at least one chip location in a test interconnect arrangement using interconnect levels close to semiconductor material in said semiconductor wafer; ~~and~~
testing at least one parameter of said subset of transistors; and
removing said test interconnect arrangement and depositing an interconnect layer of said integrated circuit in replacement thereof.
2. (original) A method according to claim 1, in which said test arrangement is constructed using only a first interconnect level above said set of transistors and the test is performed before further interconnect levels are formed.
3. (original) A method according to claim 1, in which said test arrangement is constructed using both a first and second interconnect level above said set of transistors and the test is performed before further interconnect levels are formed.
4. (currently amended) A method according to claim 1, in which said subset is a portion of ~~an~~ said integrated circuit.
5. (currently amended) A method according to claim 1, in which said subset is a subcircuit module of ~~an~~ said integrated circuit.
6. (original) A method according to claim 2, in which said subset is a subcircuit module of said integrated circuit.
7. (original) A method according to claim 1, in which said subset comprises at least two

subcircuit modules of said integrated circuit.

8. (original) A method according to claim 1, in which said test comprises providing an input test vector and recording output signals from said test structure.

9. (canceled)

10. (currently amended) A method according to claim 9 1, in which said test arrangement is constructed using only a first interconnect level above said set of transistors and the test is performed before further interconnect levels are formed.

11. (currently amended) A method according to claim 9 1, in which said test arrangement is constructed using both a first and second interconnect level above said set of transistors and the test is performed before further interconnect levels are formed.

12. (currently amended) A method according to claim 9 1, in which said subset is a portion of an said integrated circuit.

13. (currently amended) A method according to claim 9 1, in which said subset is a subcircuit module of an said integrated circuit.

14. (original) A method according to claim 10, in which said subset is a subcircuit module of said integrated circuit.

15. (currently amended) A method according to claim 9 1, in which said subset comprises at least two subcircuit modules of said integrated circuit.

16. (currently amended) A method according to claim 9 1, in which said test comprises providing an input test vector and recording output signals from said test structure.

17. (currently amended) A method of manufacturing integrated circuits with an integrated circuit process comprising the steps of:
providing a set of semiconductor wafers containing a set of chip locations for forming a set of integrated circuits therein;
fabricating a set of transistors specific to a particular integrated circuit in said wafers in said chip locations;

before electrical completion of said integrated circuit, connecting at least one subset of said set of transistors by a lithographic process in at least one chip location in a test interconnect arrangement using interconnect levels close to semiconductor material in said semiconductor wafer;
testing at least one parameter of said subset of transistors; and
modifying a step in said integrated circuit process when a parameter of said subset of transistors is out of specification; and
removing said test interconnect arrangement and depositing an interconnect layer of said integrated circuit in replacement thereof.

18. (original) A method according to claim 17, in which said test arrangement is constructed using only a first interconnect level above said set of transistors and the test is performed before further interconnect levels are formed.

19. (original) A method according to claim 17, in which said test arrangement is constructed using both a first and second interconnect level above said set of transistors and the test is performed before further interconnect levels are formed.

20. (currently amended) A semiconductor wafer containing a set of chip locations for forming a set of integrated circuits therein;
each of said set of chip locations having a set of transistors specific to a particular integrated circuit in said wafer in said chip locations, in which;
at least one chip location has a subset of transistors connected by a lithographic process in a test interconnect arrangement, different from a circuit interconnect arrangement, using interconnect levels close to semiconductor material in said semiconductor wafer, wherein
said test interconnect arrangement has been removed and replaced with an interconnect layer of said integrated circuit deposited thereon.